Claims

1.- An ultra-low power device comprising a series connection of an n-MOS transistor and a p-MOS transistor each having a source and a drain, whereby the source of the n-MOS transistor is coupled with the source of the p-MOS transistor, characterised in that the absolute values of the threshold voltages of both transistors are different, and that the absolute value of the relative difference of both threshold voltages is between 0.9 and 1.3 Volts.

2.- An ultra-low power device according to claim 1, each n-MOS and p-MOS transistor having at least one gate, whereby the gates of the n-MOS and the p-MOS transistors are coupled together thus forming a common gate.

3.- An ultra-low power device according to claim 2, whereby the common gate is coupled to ground.

4.- An ultra-low power device according to claim 2, whereby the common gate is coupled to a positive power supply.

5.- Ultra-low power circuit wherein a first and a second ultra-low power device according to claim 2 are connected together, the sources of the n-MOS and the p-MOS transistors of the first ultra-low power device being connected to the common gate of the second ultra-low power device.

6.- Ultra-low power circuit according to claim 5 wherein the drain of the p-MOS transistor of the first ultra-low power device and the drain of the p-MOS transistor of the second ultra-low power device are connected to a same potential, all transistors in the circuit being saturated in use.

7.- Ultra-low power circuit wherein a first and a second ultra-low power device according to claim 2 are connected together, the drain of the p-MOS transistor of the second ultra-low power device and the drain of the n-MOS transistor of the first ultra-low power device are connected together, and the sources of the n-MOS and the p-MOS transistors of the first ultra-low power device being connected to the common gate of the second ultra-low power device.

8.- Ultra-low power circuit wherein a first ultra-low power device according to claim 4 and a second ultra-low power device according to claim 1 are connected together, the drain of the p-MOS transistor of the first ultra-low power device and the drain of the n-MOS transistor of the second ultra-low power device being coupled together.

9.- Use of the ultra-low power device of claim 1 as a differential transconductance element able to push and/or pull current.

10.- Use of the ultra-low power device of claim 2 as a level shifter.

11.- Use of the ultra-low power device of claim 2 as a voltage reference.

12.- Use of the ultra-low power circuit of claim 8 as an operational transconductance amplifier.

13.- A diode having a first and a second terminal, the diode comprising an n-MOS transistor having a channel, a first N+ doped diffusion region at one extremity of the channel and a second N+ diffusion region at the other extremity of the channel, and a p-MOS transistor having a channel and a first P+ doped diffusion region at one extremity of the channel and a second P+ diffusion region at the other extremity of the channel,

the first N+ diffusion region of the n-MOS transistor being coupled to the first P+ diffusion region of the p-MOS transistor,

the gate of the n-MOS transistor being coupled to the second P+ diffusion region of the p-MOS transistor, and the gate of the p-MOS transistor being coupled to the second N+ diffusion region of the n-MOS transistor, and

the second P+ diffusion region of the p-MOS transistor being coupled to the first terminal of the diode and the second N+ diffusion region of the n-MOS transistor being coupled to the second terminal of the diode,

a current versus voltage characteristic of the diode being such that it has a negative slope in a reverse biased state of the diode.

14.- A diode according to claim 13, whereby the current versus voltage characteristic of the diode substantially passes through the origin of the current voltage characteristic.

15.- Voltage doubler comprising two diodes coupled in series between a supply voltage node and an output node, the anode of the first diode being coupled to the supply voltage node, and the cathode of the second diode being coupled to the output node, a clock signal switching between a first and a second voltage level being applied to the node between the cathode of the first diode and the anode of the second diode, and a load capacitance being connected to the output node, whereby the two diodes are diodes according to any of claims 13 or 14.

16.- Memory cell comprising two ultra-low power diodes according to claim 13 coupled in series reversely biased between a first low voltage level and a second high voltage level, the voltage level of the memory cell being present at the node between the two ultra-low power diodes.

17.- Use of the memory cell of claim 16 as a level holder in domino logic.

18.- Use of the memory cell of claim 16 as a level restoring device in pass gate logic.

19.- Use of the memory cell of claim 16 as a data storing device in a D latch.

20.- Use of the memory cell of claim 16 to maintain information on high impedance floating nodes in digital circuits.

21.- Use of the memory cell of claim 16 as a level keeper device in MTCMOS circuits.

22.- Electrostatic discharge protection circuit comprising a first reverse biased diode between a node to be protected and a first power supply and a second reverse biased diode between the node to be protected and a second power supply, whereby the diodes are diodes according to claim 13.

23.- Temperature independent voltage reference circuit generating a reference voltage, characterised in that it comprises a series connection of an n-MOS and a p-MOS transistor coupled with their sources together, the gates of both transistors being coupled together, the size ratio between both transistors being substantially unity, an output reference voltage of the voltage reference circuit being taken at the sources of the transistors.

24.- A temperature independent voltage reference circuit according to claim 23, characterised in that the n-MOS and the p-MOS transistor have the same channel doping level.

25.- Operational transconductance amplifier with a first input node, a second input node and an output node, characterised in that it comprises a series connection of a first series connection of a first n-MOS and a first p-MOS transistor and a second series connection of the second n-MOS and a second p-MOS transistor, the first n-MOS transistor and the first p-MOS transistor being coupled with their sources together and coupled with their gates together, thus forming a common gate coupled to a positive power supply, the drain of the first n-MOS transistor being coupled to the positive power supply,

the second n-MOS transistor and the second p-MOS transistor being coupled with their sources together, the drain of the second p-MOS transistor being coupled to the negative power supply, the gate of the second n-MOS transistor being coupled to the first input node and the gate of the second p-MOS transistor being coupled to the second input node

the drain of the first p-MOS transistor being connected to the drain of the second n-MOS transistor and to the output node,

the first n-MOS transistor and the first p-MOS transistor having a channel doping level such that the interconnection of the current characteristic in function of the gate to source voltage of both transistors happens at a positive voltage.

the first n-MOS transistor and the first p-MOS transistor having a channel doping level such that the interconnection of the current characteristic in function of the gate to source voltage of both transistors happens at a positive voltage.